Remarks

This case has been carefully considered in light of the Office Action, dated January 2, 2004, wherein: claims 1-46 were rejected under 35 USC 103(a) on Wright et al. (US Pat. No. 6,195,739 B1) in view of Tarui et al. (US Pat. No. 6,510,496 B1). Reconsideration is respectfully requested.

At the outset, the applicants respectfully submit that the rejections of claims 1-46 are based, in part, on equating "logical partitions", or "zones", with physical partitions. In particular, Tarui et al. deal with "physical partitions", while the applicants deal with "logical partitions". The confusion in the Office Action is evidenced by, for example, the statement at the end of the middle paragraph, to wit: "Furthermore, the combination of references would have provided a method capable of performing 'fault containment between (logical) partitions' and improving 'the system performance'" (see Tarui et al.; col. 2, lines 1-5). The applicants respectfully submit that insertion of the term "logical" in parentheses in the quoted statement is not correct because Tarui et al. do not deal with "logical partitions", but rather with physical partitions.

On the other hand, Wright et al. do not deal with either logical or physical partitions, but with one large operating system. Specifically, Wright et al. describe moving transient data from one stage to another in a "pipelined" processing engine. In particular, as described in Wright et al., column 9, lines 20-28:

> [A]n aspect of the processor complex architecture is the ability of the CPU 410 to operate on the transient data substantially simultaneously with the passing of that data among adjacent context memories by the data mover 450. Specifically, the context memories CMA and CMB function as ping-pong buffers by allowing the CPU core to process context data stored in one of the buffers as the other buffer is loaded with the context data received from an adjacent "upstream" processor complex.

Wright et al. thus describe a pipelined process whereby data is moved in a serial manner such that the address of the next memory location is predetermined. Wright et al. deal with the ability

to process data simultaneously with the serial movement of the data from one stage to an adjacent stage.

In contrast to the pipelined process of Wright et al., the applicants deal with movement of data among zones in a central processing complex, whereby the zone to which data is to be moved is dynamically selected, as recited by the applicants in their amended claims. The Office Action states that "the cited disclosure does not explicitly teach 'dynamically' selecting the zone of the central processing complex." The applicants agree that Wright et al. do not explicitly teach dynamic selection of the zone. Furthermore, the applicants respectfully submit that Wright et al. do not implicitly teach or even suggest dynamic selection of the zone because in Wright et al., the zone is *predetermined* as the adjacent downstream zone.

Tarui et al. do not correct the deficiency of Wright et al. with respect to dynamic selection of a zone for movement of data. Indeed, Tarui et al. do not deal with movement of data between zones of a central processing complex. In contrast, Tarui et al. deal with allocating shared memory among partitions in a multiprocessor system. Specifically, Tarui et al. provide an address management scheme, including an address translator circuit, for shared memory. In all partitions of the system, the shared memory has the same address map. (See Tarui et al., column 16, lines 43-61.) Tarui et al. provide for dynamic allocation of the shared area.

The applicants respectfully submit that the *dynamic allocation of shared memory*, as described by Tarui et al., is not equivalent to *dynamic selection of the zone in a central processing complex to which data will be moved*, as recited by the applicants in their amended independent claims 1, 18, 21, 38, 41 and 46. Although both are dynamic processes, that is where the similarity ends. In particular, as explained by Tarui et al., dynamic allocation of shared memory involves dynamic modification of the configuration information of the shared area between partitions in order to allow for flexible management of the shared area (see Tarui et al., column 3, lines 40-44). On the other hand, dynamic selection of the zone to which data is to be moved in accordance with the applicants' invention does not involve any reconfiguration of a shared area, but involves dynamically determining to which zone in a central processing complex data is to be moved.

Therefore, the dynamic allocation, or reconfiguration, of shared memory by Tarui et al. is completely different from the dynamic selection of a zone to which data is to be moved by the applicants, as recited in amended claims 1, 18, 21, 38, 41 and 46. Thus, the deficiency of Wright et al. with respect to dynamic selection, as noted in the Office Action, is not cured by Tarui et al.

The applicants thus respectfully submit that amended claims 1, 18, 21, 38, 41 and 46, and the claims dependent therefrom, are patentably distinct from the suggested combination of Wright et al. and Tarui et al. under 35 USC 103. In particular, any combination of the pipelined processing engine of Wright et al. and the shared memory multiprocessor of Tarui et al., assuming *arguendo* that they could even be combined, would not render obvious the applicants' invention , as recited, i.e., moving data between zones of a central processing complex wherein the zone to which data is to be moved is dynamically selected.

For all the foregoing reasons, reconsideration and allowance of claims 1-46, particularly as amended, are respectfully requested.

Respectfully submitted,

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